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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,197	06/07/2001	Joon-Young Yang	8733.132.20	8761

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,197	YANG, JOON-YOUNG	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/30 & 4/06/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *41-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 37 CFR 1.1 14 claiming continuation from U.S. Serial No. 09/875,197 filed on April 28, 2004 which itself claims priority under 35 U.S.C. 119(a)-(d), from Korean Patent Application No. 98-122205 filed April 07, 1998 which papers have been placed of record in the file.

Request for Continued Examination Application

The request filed on 04/28/2004 for a Request for Continued Prosecution Application (RCE) under 37 CFR 1.1 14 based on parent Application No. 09/875,197 is acceptable and a RCE has been established. An action on the RCE follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled .

The references on PTO 1499 submitted on -- -- are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 03/30 /04 and 04/06/2004 which was entered on April 28, 2004 therefore claims 41 to 56 as recited in the amendment of 04/06/2004 are currently pending in the application.

Claims 41 and 55 have been amended by the amendment of April 06, 2004.

Specification

The disclosure is objected to because of the following informalities: Applicant cooperation is appreciated to correct the numerous error in specification and claims due to a translation into English from a foreign document which contains grammatical and idiomatic errors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (U.S. Patent No. 5,897,346, herein after Yamamguchi) previously applied and in view of Aomori et al. (U.S. Patent No. 5,504,020, herein after Aomori)..

With respect to claim 41 Yamaguchi describes a method of fabricating a thin film transistor, comprising: forming a gate insulating layer on an active layer (Yamaguchi fig.

1B # 13, col. 8 line2 and fig. 1C # 14); forming a gate on the gate insulating layer; forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask (figs. 1 C and A); and forming an impurity region by heavily implanting impurity ions to said excited region in a heavy dosage while the excited region remains in an excited state, (Fig. 1 C implanting P+ ions Yamaguchi col. 9 lines 14 and figs. 1C, etc. describe heavily implanting ions,).

(It is noted that Yamaguchi discloses the use of active layer as a mask and implanting prior to the formation of the gate. However it would be an obvious altering of the sequence of steps to implant the H after gate formation. Further as Applicants' claims use the terminology " comprising" the claim includes steps in any sequence) .

Yamaguchi does not specifically disclose the presently newly added limitation namely , "whereby impurity ions become self-activated".

However , Aomori, a patent from the same filed of endeavor, describes in col.3 lines 13 to 25 ion shower doping method wherein heavy doping/implantation of Hydrogen ions the impurity ions are self-activated in the polycrystalline thin film to fabricate TFTs at low temperature thereby allowing the use of low temperature melting materials to be used and to control the precise amount of Hydrogen to be implanted is attained thereby a TFT with higher reliability is obtained.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Aomori's step of heavy ion doping which causes the impurity ions to be self-activated in Yamaguchi's method. the motivation to include Aomori's afore mention steps in to Yamaguchi's method are to fabricate TFTs at low temperature

thereby allowing the use of low temperature melting materials to be used and to control the precise amount of Hydrogen to be implanted is attained thereby a TFT with higher reliability is obtained. (Aomori col. 2 and col. 4 lines 20 to 55).

With respect to claim 42 Yamaguchi describes the method of claim 41, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate. (Yamaguchi col. 8 line 2).

With respect to claim 43 Yamaguchi describes t he method of claim 41, wherein the active layer is formed by depositing undoped polycrystalline silicon. (Yamaguchi col. 7 line 50).

With respect to claim 44 , Yamaguchi describes the method of claim 43, wherein the undoped polycrystalline silicon has a thickness of between about 400 and 800 A. (Yamaguchi col. 7 line 47).

With respect to claim 45 Yamaguchi describes the method of claim 43, wherein the active layer is formed using chemical vapor deposition process. (Yamaguchi col. 7 line 48)

With respect to claim 46 Yamaguchi describes the method of claim 41, wherein the active layer is formed by depositing amorphous silicon and crystallizing the amorphous silicon by laser annealing. (Yamaguchi col. 7 lines 46-51).

With respect to claim 47, Yamaguchi describes the method of claim 41, wherein the exposed portion of the active layer is formed by the steps of depositing an another layer of silicon dioxide on the gate insulating layer to cover the active layer; depositing a

conductive material on the another layer of silicon dioxide; and patterning the conductive material and the another layer of silicon dioxide to form an insulating layer and to form the gate over a selected portion of the active layer. (Yamaguchi Fig. 3 E).

With respect to claim 48 Yamaguchi describes the method of claim 47, wherein the gate insulating layer and the gate comprise a thickness of about 500-1500 A and, about 1500-:2500 A, respectively. (Yamaguchi col. 8 lines 2 and 5).

With respect to claim 49 Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted with implantation energy between about 50 and 150 KeV. (Yamaguchi col. 9 line 15).

With respect to claim 50 Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted with a dose of between about 5×10^{14} - 5×10^{16} ions/cm^2 (Yamaguchi col. 9 line 14).

With respect to claim 51 Yamaguchi describes the method of claim 49, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius. (Yamaguchi col.9 line 15 and 54).

With respect to claim 52 Yamaguchi describes the method of claim 50, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius. (Yamaguchi col.9 line 15 and 54).

With respect to claim 53, Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted in the active layer and simultaneously form the impurity region. (It is inherent when a dopant is implanted an impurity region is formed).

With respect to claim 54, Yamaguchi describes the method of claim 41, wherein the hydrogen ion implantation time is proportionately related to the size of the active layer. (Inherent because bigger the area the longer it will take).

With respect to claim 55, Yamaguchi describes a thin film transistor prepared by a process comprising: forming a gate insulating layer on an active layer; forming a gate on the gate insulating layer; forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask; and forming an impurity region by implanting impurity ions to said excited region while the excited region remains in an excited state, wherein the activation of said impurity ions implanted heavily occurs as the step of said implanting impurity ions is performed. (rejected for same reasons as claim 41 above).

Wit respect to claim 56 Yamaguchi describes the thin film transistor of claim 55, wherein the, gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate, and the active layer is formed by depositing undoped polycrystalline silicon. (rejected for same reasons as claim 42).

Response to Arguments

Applicant's arguments with respect to claims 41-56 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

June 25, 2004.

LONG PHAM
PRIMARY EXAMINER